

**WHAT IS CLAIMED IS:**

1           1. A signal receiver for receiving a differential input  
2 signal pair through an external differential input terminal  
3 pair, comprising:

4           a positive feedback differential amplifier having a  
5 differential input terminal pair and a differential output  
6 terminal pair;

7           a coupling circuit, coupled to the external differential  
8 input terminal pair, the differential input terminal pair and  
9 the differential output terminal pair, for coupling the  
10 differential input signal pair on the external differential  
11 input terminal pair to the differential input terminal pair;  
12 and

13           a pre-charger for pre-charging the differential input  
14 terminal pair to a predetermined voltage level;

15           wherein the differential input terminal pair is coupled  
16 to the external differential input terminal pair before a  
17 first time point, the differential input signal pair enters  
18 into the differential input terminal pair of the positive  
19 feedback differential amplifier via the coupling circuit  
20 after the first time point, and the positive feedback  
21 differential amplifier is activated to amplify the entered  
22 differential input signal pair and outputs to the  
23 differential output terminal pair at a second time point a  
24 predetermined period after the first time point.

1           2. The signal receiver as claimed in claim 1, wherein  
2 the coupling circuit includes a first coupling circuit and a

3 second coupling circuit, the first coupling circuit  
4 comprising:

5 a first transistor of a first type; and

6 a second transistor of a second type, wherein the gates  
7 of the first transistor and the second transistor are coupled  
8 to a first terminal of the differential output terminal pair,  
9 sources of the first transistor and the second transistor are  
10 coupled to a first terminal of the differential input  
11 terminal pair, and a drain of the first transistor serves as  
12 a first terminal of the external differential input terminal  
13 pair;

14 and the second coupling circuit comprising:

15 a third transistor of the first type; and

16 a fourth transistor of the second type, wherein gates of  
17 the third transistor and the fourth transistor are coupled  
18 together to a second terminal of the differential output  
19 terminal pair, sources of the third transistor and fourth  
20 transistor are coupled together to a second terminal of the  
21 differential input pair, and a drain of the third transistor  
22 serves as a second terminal of the external differential  
23 input terminal pair.

1 3. The signal receiver as claimed in claim 2, wherein  
2 the first type transistors are PMOS transistors, the second  
3 type transistors are NMOS transistors, and drains of the  
4 second transistor and the fourth transistor are connected to  
5 the ground.

1 4. The signal receiver as claimed in claim 2, wherein  
2 the first type transistors are PMOS transistors, the second

3 type transistors are NMOS transistors, and drains of the  
4 second transistor and the fourth transistor are connected to  
5 a high voltage.

1 5. The signal receiver as claimed in claim 1, wherein  
2 the coupling circuit includes a first coupling circuit and a  
3 second coupling circuit, the first coupling circuit  
4 comprising:

5 a first capacitor having a first end coupled to a first  
6 terminal of the external differential input terminal pair;  
7 and

8 a fifth transistor having a gate connected to a first  
9 terminal of the differential output terminal pair, and a  
10 drain connected to a second end of the first capacitor and a  
11 first terminal of the differential input terminal pair;

12 and the second coupling circuit comprising:

13 a second capacitor having a first end coupled to a  
14 second terminal of the external differential input terminal  
15 pair; and

16 a sixth transistor having a gate connected to a second  
17 terminal of the differential output terminal pair, and a  
18 drain connected to a second end of the second capacitor and a  
19 second terminal of the differential input terminal pair.

1 6. The signal receiver as claimed in claim 5, wherein  
2 the fifth transistor and the sixth transistor are NMOS  
3 transistors having sources connected to the ground.

1 7. The signal receiver as claimed in claim 5, wherein  
2 the fifth transistor and the sixth transistor are PMOS

transistors, having their sources connected to a high voltage.

8. The signal receiver as claimed in claim 1, wherein the pre-charger comprises:

a first local control transistor having a gate connected to a first control signal for pre-charging a first terminal of the differential input terminal pair to the predetermined voltage level before the first time point, the first local control transistor being turned off after the first time point; and

a second local control transistor having a gate connected to the first control signal for pre-charging a second terminal of the differential input terminal pair to the predetermined voltage level before the first time point, the second local control transistor being turned off after the first time point;

wherein the external differential input terminal pair are pre-charged to the predetermined voltage level before the first time point and the positive feedback differential amplifier is controlled with a second control signal for defining the second time point.

9. The signal receiver as claimed in claim 1, wherein the pre-charger comprises:

a third local control transistor having a gate connected to a second control signal, and a source and a drain connected to the differential output terminal pair, wherein the second control signal is used for defining the second time point.

1           10. A signal receiver for receiving an independent input  
2 signal via an external input terminal, comprising:

3           a positive feedback differential amplifier having a  
4 differential input terminal pair and a differential output  
5 terminal pair;

6           a coupling circuit, coupled to the external input  
7 terminal, the differential input terminal pair and the  
8 differential output terminal pair, for coupling the  
9 independent input signal on the external input terminal to  
10 the differential input terminal pair; and

11          a pre-charger for pre-charging the differential input  
12 terminal pair to a predetermined voltage level;

13          wherein one of the differential input terminal pair is  
14 coupled to the external input terminal before a first time  
15 point, wherein the independent input signal enters the  
16 differential input terminal pair of the positive feedback  
17 differential amplifier via the coupling circuit after the  
18 first time point, and the positive feedback differential  
19 amplifier is activated to amplify the entered independent  
20 input signal and outputs to the differential output terminal  
21 pair at a second time point a predetermined period after the  
22 first time point.

1           11. The signal receiver as claimed in claim 10, wherein  
2 the coupling circuit includes a first coupling circuit and a  
3 second coupling circuit, the first coupling circuit  
4 comprising:

5           a first capacitor having a first end coupled to the  
6 external input terminal; and

7 a first transistor having a gate connected to a first  
8 terminal of the differential output terminal pair, and a  
9 drain connected to a second end of the first capacitor and a  
10 first terminal of the differential input terminal pair;

11 and the second coupling circuit comprising:

12 a second capacitor having a first end connected to a  
13 fixed voltage level; and

14 a second transistor having a gate connected to a second  
15 terminal of the differential output terminal pair, and a  
16 drain connected to a second end of the second capacitor and a  
17 second terminal of the differential input terminal pair.

1 12. The signal receiver as claimed in claim 11, wherein  
2 the first transistor and the second transistor are NMOS  
3 transistors having sources connected to the ground.

1 13. The signal receiver as claimed in claim 11, wherein  
2 the first transistor and the second transistor are PMOS  
3 transistors having sources connected to a high voltage.

1 14. The signal receiver as claimed in claim 10, wherein  
2 the pre-charger comprises:

3 a first local control transistor having a gate connected  
4 to a first control signal for pre-charging a first terminal  
5 of the differential input terminal pair to the predetermined  
6 voltage level before the first time point, the first local  
7 control transistor being turned off after the first time  
8 point; and

9 a second local control transistor having a gate  
10 connected to the first control signal for pre-charging a

11 second terminal of the differential input terminal pair to  
12 the predetermined voltage level before the first time point,  
13 the second local control transistor being turned off after  
14 the first time point;

15 wherein the external input terminal is pre-charged to  
16 the predetermined voltage level via the coupling circuit  
17 before the first time point and the positive feedback  
18 differential amplifier is controlled with a second control  
19 signal for defining the second time point.

1 15. A signal transmitter for transmitting a differential  
2 input signal pair to a transmission line via an external  
3 differential output terminal, comprising:

4 a control circuit, controlled by a first control signal  
5 for defining a first time point, for pre-charging the  
6 transmission line to a predetermined voltage level via the  
7 external differential output terminal before the first time  
8 point, and transmitting the differential input signal pair to  
9 the transmission line after the first time point.

1 16. The signal transmitter as claimed in claim 15,  
2 wherein the control circuit is a differential circuit coupled  
3 to the external differential output terminal and controlled  
4 by the first control signal, wherein the differential circuit  
5 has a dynamic load controlled by the first control signal for  
6 pre-charging the transmission line to the predetermined  
7 voltage level.

1 17. The signal transmitter as claimed in claim 15,  
2 wherein the control circuit is a differential circuit coupled

3 to the external differential output terminal and controlled  
4 by the first control signal, wherein the differential circuit  
5 has a fixed load for pre-charging the transmission line to  
6 the predetermined voltage level.

1 18. The signal transmitter as claimed in claim 15,  
2 wherein the control circuit includes:

3 a first logic gate having an input terminal pair coupled  
4 to the first control signal and a first signal of the  
5 differential input signal pair, and an output terminal  
6 coupled to a first terminal of the external differential  
7 output terminal, for pre-charging a first path of the  
8 transmission line to the predetermined voltage level via the  
9 first terminal of the external differential output terminal  
10 before the first time point, and substantially transmitting  
11 the first signal of the differential input signal pair to the  
12 first path of the transmission line after the first time  
13 point; and

14 a second logic gate having an input terminal pair  
15 coupled to the first control signal and a second signal of  
16 the differential input signal pair, and an output terminal  
17 coupled to a second terminal of the external differential  
18 output terminal, for pre-charging a second path of the  
19 transmission line to the predetermined voltage level via the  
20 second terminal of the external differential output terminal  
21 before the first time point, and substantially transmitting  
22 the second signal of the differential input signal pair to  
23 the second path of the transmission line after the first time  
24 point.



1 19. The signal transmitter as claimed in claim 18,  
2 wherein the first logic gate and the second logic gate are  
3 NAND gates.

1 20. The signal transmitter as claimed in claim 18,  
2 wherein the first logic gate and the second logic gate are  
3 NOR gates.

1 21. The signal transmitter as claimed in claim 15,  
2 wherein the control circuit substantially cuts off the  
3 interconnection between the differential input signal pair  
4 and the transmission line within a predetermined period after  
5 the first time point.

1 22. The signal transmitter as claimed in claim 21,  
2 wherein the control circuit includes:

3 a first differential circuit having an input terminal  
4 pair connected to the first control signal and the external  
5 differential output terminal, and an output terminal pair for  
6 outputting a feedback signal pair; and

7 a second differential circuit having an input terminal  
8 pair connected to the first control signal, the differential  
9 input signal pair and feedback signal pair, and an output  
10 terminal pair connected to the external differential input  
11 terminal.

1 23. The signal transmitter as claimed in claim 21,  
2 wherein the control circuit comprises:

3 a first logic gate having an input terminal connected to  
4 the first control signal, a first signal of the differential

5 input signal pair and a first feedback signal, and an output  
6 terminal connected to a first terminal of the external  
7 differential output terminal;

8 a second logic gate having an input terminal connected  
9 to the first control signal, a second signal of the  
10 differential input signal pair and a second feedback signal,  
11 and an output terminal connected to a second terminal of the  
12 external differential output terminal;

13 a third logic gate having an input terminal connected to  
14 the first control signal and the first terminal of the  
15 external differential output terminal, and an output terminal  
16 for outputting the first feedback signal; and

17 a fourth logic gate having an input terminal connected  
18 to the first control signal and the second terminal of the  
19 external differential output terminal, and an output terminal  
20 for outputting the second feedback signal.

1 24. The signal transmitter as claimed in claim 23,  
2 wherein the first logic gate, the second logic gate, the  
3 third logic gate and the fourth logic gate are NAND gates.

1 25. A signal transmission system, mounted into a chip  
2 and having a signal transmitter and a signal receiver  
3 connected with each other by a transmission line, wherein the  
4 signal transmitter transmits a differential input signal pair  
5 to the transmission line via an external differential output  
6 terminal pair and the signal receiver receives the  
7 differential input signal pair via the external differential  
8 input terminal pair, the signal transmitter comprising:

9 a control circuit, controlled by a first control signal  
10 for defining a first time point for pre-charging the  
11 transmission line to a predetermined voltage level via the  
12 external differential output terminal pair before the first  
13 time point, and substantially transmitting the differential  
14 input signal pair to the transmission line after the first  
15 time point;

16 and the signal receiver comprising:

17 a positive feedback differential amplifier having a  
18 differential input terminal pair and a differential output  
19 terminal pair;

20 a coupling circuit, coupled to the external differential  
21 input terminal pair, the differential input terminal pair and  
22 the differential output terminal pair, for coupling the  
23 differential input signal pair on the external differential  
24 input terminal pair to the differential input terminal pair;  
25 and

26 a pre-charger for pre-charging the differential input  
27 terminal pair to the predetermined voltage level;

28 wherein the differential input terminal pair is coupled  
29 to the external differential input terminal pair before the  
30 first time point, wherein the differential input signal pair  
31 enters the differential input terminal pair of the positive  
32 feedback differential amplifier via the coupling circuit  
33 after the first time point, and the positive feedback  
34 differential amplifier is activated to amplify the entered  
35 differential input signal pair and outputs to the  
36 differential output terminal pair at the second time point a  
37 predetermined period after the first time point.

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